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Claims

[c1] 1.A circuit for programming and testing electrical fuse (eFuse) circuits in a device, said circuit comprising:
an eFuse circuit that includes a fuse, a blow device, and a control input for said blow device;
a first circuit capable of determining when to blow said fuse; and
a second circuit capable of triggering a bypass of a pre-blow process within said eFuse circuit when said fuse is not to be blown, wherein a shifted 1 propagating through a plurality of eFuse circuits within said device is passed to a next downstream eFuse circuit without delay attributable to said pre-blow process.

[c2] 2. The circuit of Claim 1, wherein said first circuit comprises:
a first latch component having multiple inputs and which provides a true output;
a second latch component having multiple inputs and which provides both a second true output and a complement output;
wherein said second latch component is programmed with a blow value for said fuse such that the blow value

dictates when a fuse is to be blown; and
a program signal that together with said true output and said second true output provides the control input to said blow device.

[c3] 3. The circuit of Claim 2, wherein said program signal is an EFUSEPROGRAM (EFP) signal.

[c4] 4. The circuit of Claim 1, wherein said second circuit comprises:
an AND gate having a first input coupled to said complement output of said second latch, a second input coupled to said program signal, and a result output;
a multiplexer (MUX) having a first MUX input coupled to the true output of said first latch component, a second MUX input coupled to a selected output of a previous MUX of a third eFuse circuit sequentially before said eFuse circuit, a select input coupled to said result output of said AND gate, and a select output.

[c5] 5.The circuit of Claim 4, wherein further:
said first MUX input is selected when said result output is low (0);
said second MUX input is selected when said result output is high (1); and
said blow device is triggered to blow said fuse when said first MUX input is selected and both said true output and

said second true output are high.

[c6] 6. In a device that includes multiple, serially connected, electrical fuse (eFuse) circuits, a system for programming and testing eFuse circuits, said system comprising:
an AND gate having two inputs and a result output;
a multiplexer (MUX) having a first input, a second input, a select input, and a MUX
output, wherein select input is coupled to said result output of said AND gate;
wherein, said eFuse circuit includes a fuse coupled to a switch that is controlled by
signals from a fuse latch, a pattern latch, and a program signal source, said pattern latch being programmed with a fuse blow status indicating whether or not said fuse is to be blown during device testing; and
an enabling circuit capable of enabling a bypass of a pre-blow process within said eFuse circuit when said fuse blow status indicates that said fuse is not to be blown, such that a time delay associated with said fuse-blow process is substantially eliminated as a testing operation proceeds to each eFuse circuit within said device.

[c7] 7. The system of Claim 6, wherein said enabling circuit includes connecting components and signals of said eFuse circuit to said MUX and said AND gate, wherein said MUX and said AND gate provide a bypass function

that determines when a shifted "1" that is being serially propagated to each of said eFuse circuits should be forwarded to said fuse latch for initiating a blow of said fuse, wherein when a fuse blow status within said pattern latch indicates that said fuse is not to be blown, said MUX forwards said shifted 1 to a next eFuse circuit without waiting on a completion of said pre-blow process.

[c8] 8. The circuit of Claim 6, wherein:
a first input of said AND gate is coupled to a complement of a signal from said pattern latch indicating the fuse blow status;
a second input of said AND logic is coupled to said program signal source;
said first input of said MUX is coupled to said fuse latch; and
said second input of said MUX is coupled to a MUX output of a previous MUX.

[c9] 9. The system of Claim 8, wherein further said MUX output of said MUX is connected to a second input of a next MUX of a next eFuse circuit.

[c10] 10. The system of Claim 7, wherein said second input of said MUX is coupled to a fuse in signal when said MUX is a first MUX in said serially connected eFuse circuits.

[c11] 11. The system of Claim 6, wherein, said eFuse circuit is a first eFuse circuit that is
serially connected to a second eFuse circuit, whose fuse blow status indicates its fuse should not be blown, and a third eFuse circuit whose fuse blow status indicates its fuse should be blown, said circuit comprising:
a routing circuit capable of routing said shifted 1 through said fuse latch of said first eFuse circuit, subsequently bypassing a fuse latch of said second eFuse circuit, and then routing said shifted 1 through a fuse latch of said third eFuse circuit, wherein only said first eFuse circuit and said third eFuse circuit utilizes processing time for routing said shifted 1 through respective fuse latches before forwarding said shifted 1 to a next eFuse circuit.

[c12] 12.In a device that includes multiple, serially connected eFuse circuits, each having a
fuse, a fuse switch, a fuse latch, a pattern latch, a fuse program signal, AND logic and a bypass multiplexer (MUX), a method for reducing programming and testing time for said device comprising:
storing a fuse blow status within said pattern latch;
ANDing a complement of said fuse blow status with said fuse program signal;
selecting one of two inputs of said MUX based on a re-

sult of said ANDing step, said inputs including a first input coupled to a true output of said fuse latch and a second input coupled to a MUX output of a previous eFuse circuit;

forwarding a shifted 1 propagating through said device to a next eFuse circuit without waiting for a pre-blow processing time to elapse when said second input is selected, wherein a time delay for propagating said shifted 1 through said eFuse circuit is substantially eliminated.